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A CO-DESIGN METHODOLOGY FOR SYSTEM INTERCONNECT

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1 OVERVIEW

Every electronics manufacturer races new products to market to the same mantra: smarter, faster, less expensive, and more reliable. The trouble is these high performance products require complex designs that create unprecedented technical challenges driven by density, speed, and power. These challenges are manifested in physical design, signal integrity, timing, and power delivery issues, creating problems that, if not readily resolved, can impact a manufacturer's profitability.

The solution comes in the form of a change in design methodology for electronic systems and a change in design chain management. The first—a change in the way products are designed—is revolutionary. Electronic systems are going to be designed at the same time, across the domains of integrated circuits (ICs), IC packages, and printed circuit boards (PCBs). The second—design chain management—will now be integrated into the design process to reduce cost of goods sold and design support costs while improving productivity across the entire design chain.

This paper outlines a new co-design methodology that enables design and analysis of the electronic system interconnect from IC to IC, across packages, connectors, backplanes, and PCBs. Supported by a unique technology platform, the new methodology enables engineers to co-design an IC, its package, and its PCB, optimizing the system interconnect. Many companies will be able to remove weeks or months from the design process with the combination of best practices and deployment of the proposed co-design methodology and associated technology platform.

2 SYSTEM INTERCONNECT DEFINED

The term *system interconnect* refers to the logical, physical, and electrical connection of a signal, its associated return path, and its power delivery system.

The system interconnect travels from an IC I/O buffer through a bump and package substrate to a package pin, across a printed circuit board and connector, back through another PCB, to a package pin and through a package substrate and bump, to another IC I/O buffer (*see Figure 1*). Currently, the system interconnect is designed and implemented sequentially across the domains of IC, IC packaging, and PCB in a relatively long and costly process.

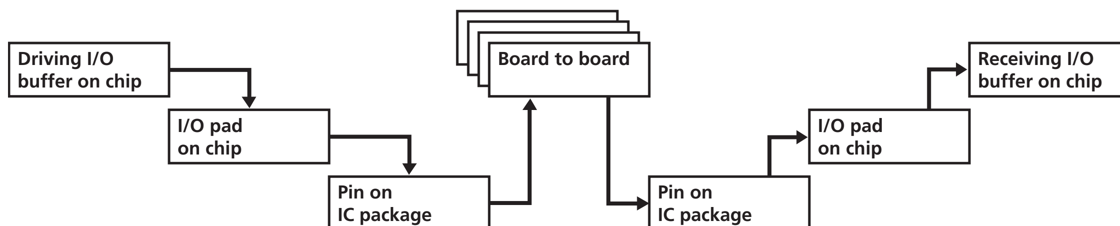

Figure 1: The system interconnect is designed across the domains of IC, IC package, and PCB

3 MARKET DRIVERS FOR SYSTEM INTERCONNECT DESIGN

Today, IC manufacturers and systems companies are dealing with raised market expectations and shrinking market opportunity windows. Advances in engineering and manufacturing, as well as globalization of markets, have led consumers to expect low-cost, high-quality, high-performance products. Time-to-market is critical. To remain competitive, manufacturers have to find ways to reduce design cycle times and costs. Improving design of system interconnects can help them to achieve those goals through the following results:

- Elimination of design iterations between the IC, IC package, and PCB design domains and reduction of design cycles within the domains.
- Additionally, IC and IC packaging companies can realize these benefits:
  - Reduction and even elimination of the risk of IC mask re-spins. It can take six to eight weeks to re-do the re-distribution layer (RDL) of an IC, while a new mask can run $50,000
  - Improved time-to-volume for new devices through the use of innovative silicon design-in kit technology. Systems companies can now quickly design-in a new, complex IC
  - Reduction in the cost of the IC package and elimination of package re-spins by enabling use of a standard package. The package is usually the most expensive component of a finished IC and a custom package will be three times more expensive than a standard, off-the-shelf package

- Systems companies can also benefit from the following:
  - A constraint-driven high-speed PCB flow that allows first time design success, eliminating costly prototype board spins
  - An integrated high-speed analysis solution that helps quickly develop optimal constraints, shaving weeks or months off the design cycle
  - Silicon design-in kit technology that can cut eight to twelve weeks from a design cycle, shortening time-to-market

4 TECHNICAL TRENDS AND CHALLENGES IN SYSTEM DESIGN

The economics of system design are tightly tied to the technical challenges. The proliferation of high-performance ICs, high-speed systems, increased power demands, and complex packaging techniques have created monumental design challenges driven by density, speed, and power.

4.1 DENSITY: IC PACKAGING GETS MORE COMPLEX

Density of interconnect will continue to escalate as illustrated below. Both IC I/Os and the number of pins on a PCB are increasing at a rapid clip. At the same time, the average PCB size is decreasing, resulting in much denser interconnect on the IC package and PCB. Higher density increases the likelihood of crosstalk, more discontinuities in the signal path and power delivery, and underscores that it's just plain difficult to physically implement more interconnect in less space.

Mid-range to high-performance systems

		2002-2003	2004-2005	2006-2007	2008-2012
Max pins/component	count	480-800	520-1000	640-1600	1200-1800
Pins/board	count k	21-115	27-144	34-225	38-225
Board size	sq. cm	500-1500	450-1200	400-1000	300-800
Cost/interconnect	$	0.05-0.18	0.06-0.16	0.07-0.14	0.06 0.13

Source: IPC National Technology Roadmap for Electronic Interconnections 2002/2003

Table 1: Density of interconnect continues to escalate

On the IC packaging front, designers are employing new and innovative techniques to deal with the high I/O densities, increased signals, and tighter geometries of nanometer-scale devices. System-on-a-chip (SoC) designs demand higher integration, resulting in high packaging pin counts and density. High frequency designs require complicated flip-chip technologies to avoid the high inductance of wirebond. Stacked-die and stacked-wire packages are increasing in popularity as they save valuable board real estate, but require management of hundreds—or thousands—of stacked wirebonds. System-in-package (SiP) technology provides a means of integrating complete systems on a common substrate and proves a viable alternative to more costly SoCs, but brings integration challenges of its own. *Figure 2* illustrates a variety of packaging techniques all within a single SiP.

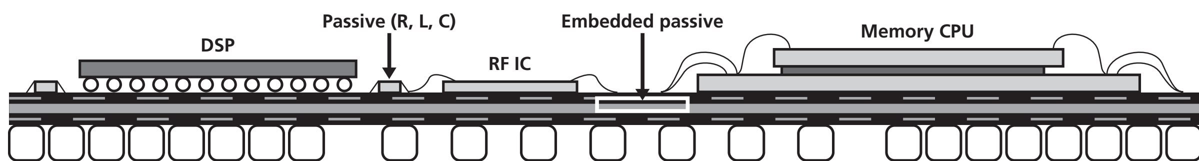

Figure 2: Packaging technologies are constantly evolving as designers endeavor to keep up with the need for faster ICs and smaller products

4.2 SPEED: HIGH-SPEED PCB INTERFACES

As PCB system data rates move into the gigahertz range (*see Figure 3*), designers are challenged to ensure signal integrity, reliable timing, adequate power distribution, and to achieve successful multilayer routing. Signal integrity and power delivery emerge as key issues that must be resolved. Board topologies for common communication formats must be modeled carefully and repeated from design to design for efficiency.

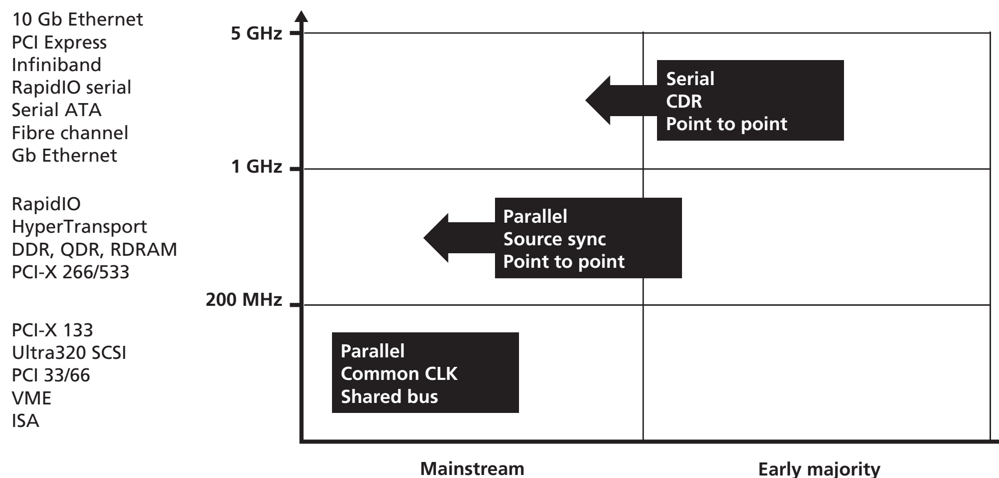

Figure 3: Data rates are moving into the multigigahertz range, requiring new approaches to the modeling and analysis of system interconnects to avoid signal integrity and power delivery issues

4.3 POWER: NO LONGER AN AFTERTHOUGHT

Over the past decade, power delivery requirements for high-speed systems have increased rapidly while supply voltages have dropped. As can be seen below, IC I/Os are getting faster and voltages are decreasing while power consumption is accelerating, leading to tighter noise margins.

Mid-range to high-performance systems

		2002-2003	2004-2005	2006-2007	2008-2012
Rise time (ns)	ns	0.8-0.3	0.6-0.2	0.5-0.2	0.4-0.1
Min device voltage	v	2.0-2.8	1.8-2.5	1.5-2.0	1.2-1.2
Voltage levels	count	3-5	2-5	2-5	2-5
Frequency on board	MHz	350-800	450-900	500-1000	750-1200
Power dissipation	W	20-90	50-100	70-110	80-150

Source: IPC National Technology Roadmap for Electronic Interconnections 2002/2003

Table 2: Faster ICs, decreased voltages, and increasing power consumption are resulting in tighter noise margins

At the same time, the number of power feeds to a single complex IC requires the careful design of power delivery and return paths. An IC, for example, may require different power supplies for its serial I/O, parallel I/O, termination, and analog circuits. Each power distribution system needs to be designed individually, significantly impacting floorplanning and routing of the IC package and PCB.

5 DESIGNING THE SYSTEM INTERCONNECT TODAY

At present, design and analysis of the system interconnect is performed using a highly fragmented set of design processes across three dissimilar design domains: IC, IC packaging, and PCB. Each design domain employs separate development processes, with final resolution of design issues being handled by the system designer at the integration phase. These development processes are only loosely coupled by paper specification and spreadsheets that are managed outside of the implementation flows, resulting in an inefficient and error-prone practice.

The problems in designing a high-speed system interconnect become apparent when we consider how each of the design domains contribute to the development of the system interconnect using today's methodologies.

5.1 THE IC DESIGN ENVIRONMENT

Often, IC designers don't consider the IC package or the PCB system in their design. Their view of the system interconnect—the interconnect from IC I/O buffer through a bump and package substrate to a package pin—causes them to treat the PCB and sometimes the package, if they don't have the data, as an ideal load condition. To ensure a successful design, they often have to minimize risk by over-designing

the IC, incurring unnecessary costs and leaving performance on the design table. Yet another missed opportunity involves the placement of the bumps on the die. While many factors influence the placement of the I/O buffers and the bumps, the IC designer does have some flexibility through the definition of the RDL to optimize bump placement in order to simplify IC package design, both electrically and physically.

5.2 THE IC PACKAGING DESIGN ENVIRONMENT

Although IC packaging is a critical link in the system design process, most IC package designers don't have enough information early enough from either the IC designer or the PCB designer to optimize a package for the system. This lack of visibility can result in several re-spins of the package if the IC does not work as intended. Or, even worse, if the problem can't be fixed in the package, re-spins of the IC RDL mask may be required — a very expensive proposition. On the board side, a lack of foresight of the IC and its package by the IC packaging designer can result in a more difficult and time-consuming board design, a more expensive board design, or even an impossible board design. Without good package design, the board designer is unable to optimize the layout so that the signals fanout correctly on the board for routability with minimum crossovers of connections and a minimal number of vias.

5.3 THE PCB DESIGN ENVIRONMENT

The PCB design environment has advanced considerably to effectively execute high-speed designs. In a high-end, integrated design environment, engineers can explore, design, implement, and verify PCB designs. The problem is, PCB design flows focus only on the PCB interconnect — that is the interconnect from package pin, across a printed circuit board and connector, back through another PCB, to a package pin. To a PCB designer, the rest of the interconnect is a black box (an electronic component whose circuitry is unknown, but whose function is understood). So, as good as today's PCB tools may be, most designers can only optimize the interconnect for the PCB piece of the design. This approach is a missed opportunity to make system level trade-offs. For example, at a higher level, timing skews on the IC package could be compensated for on the PCB, increasing margins and loosening constraints.

5.4 ENVISIONING A CO-DESIGN METHODOLOGY FOR SYSTEM INTERCONNECT

Aware that the isolated processes they have been using are not doing the job, engineers are looking for new solutions. They now need to expand their focus to the entire system interconnect. Timing margins alone are demanding a change; margins are now so tight they need to be managed across all three domains to ensure success. Unfortunately, there is little EDA-supported methodology for the design and analysis of the interconnect across domains. What is needed is a new "co-design" approach capable of supporting complete modeling and analysis of the system interconnect across the IC, its package, and the PCB. Such a solution would reduce design times and design costs and avoid costly re-spins.

6 A SYSTEM INTERCONNECT CO-DESIGN METHODOLOGY

The new co-design methodology proposed here will enable all of the players involved in the design process to model and analyze the design and implementation of system interconnects from specification through manufacturing. *Figure 4* shows the co-design workflow and indicates interactions between various team members.

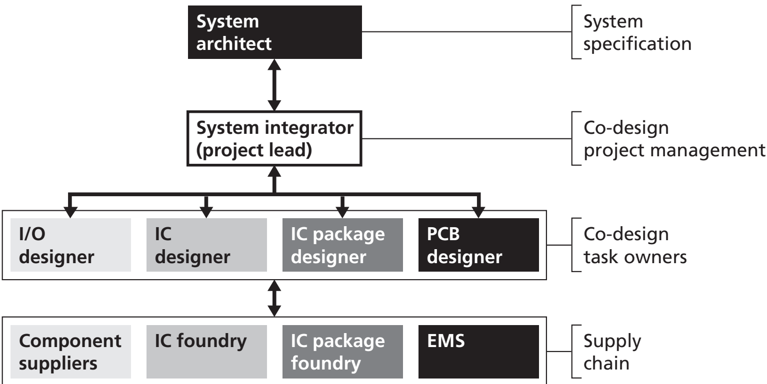

Figure 4: Designers involved in electronic system interconnect design can collaborate within one company or across several companies that are often part of the same supply chain

Importantly, the co-design methodology captures and links the design processes for the three design domains. It is capable of addressing any of these possible design scenarios:

- A new design of IC, package, and PCB;
- A package-driven design in which the IC package is constrained and the IC has to work within those constraints, i.e. a cost reduction of an existing IC requires “plug-and-play” with pre-existing boards;
- A PCB-driven design in which the IC and package need to satisfy board-level constraints as in PC architectures that require ICs to be configured in such a way that they can implemented successfully on the motherboard

6.1 A NEW APPROACH TO SYSTEM INTERCONNECT DESIGN

The new system interconnect co-design methodology begins with the understanding that “design” is a convergent process, starting with an abstract model at specification and maturing into manufactured components. Accordingly, at the heart of the new methodology is a process for creating an abstract or virtual system interconnect model (VSIC model) that will serve to validate the feasibility of the initial system specification. The VSIC model is used to describe the physical, logical, and electrical properties of the system interconnect including the corresponding power delivery system. It is, in essence, a topology that describes the entire interconnect. It can be used to capture and validate certain design assumptions and specifications and can be matured throughout the design process.

Figure 5 shows how team members can test the VSIC model and feed back information to the system integrator about the viability of the design. Any necessary trade-offs can then be made and the VSIC model updated.

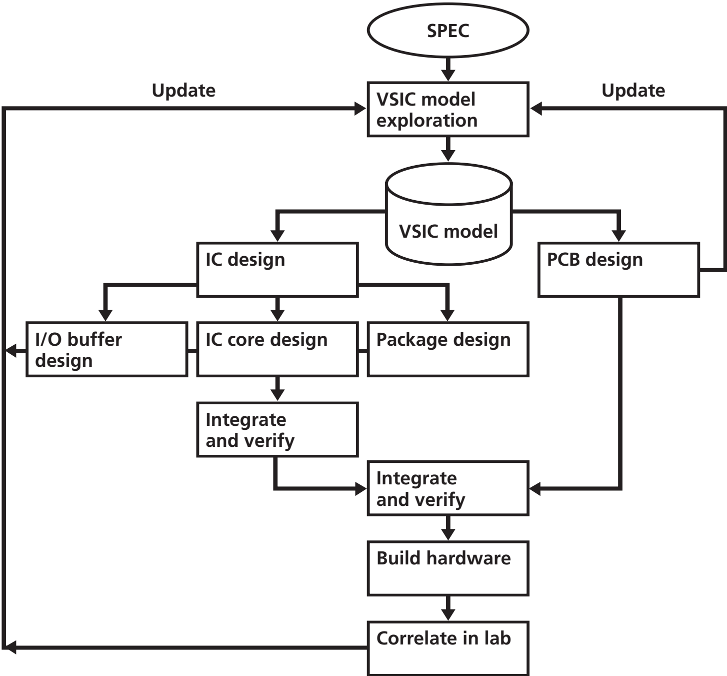

Figure 5: A VSIC model drives a true co-design methodology

6.2 A CLOSER LOOK AT THE SYSTEM INTERCONNECT

Referencing our earlier description of system interconnect (Section 2), the VSIC model will have at least five segments: buffer to bump, bump to package pin, package pin to package pin, package pin to bump, and bump to buffer.

Figure 6 illustrates a differential interconnect for a single signal. Of course, a high-speed system will consist of a number of such signals—there will be multiple ICs connected together by multiple interconnects as needed by buses, serial interfaces, and other single ended connections. For discussion purposes, however, we will focus on one piece of interconnect and assume this methodology will be applied to all of the high-speed interconnect.

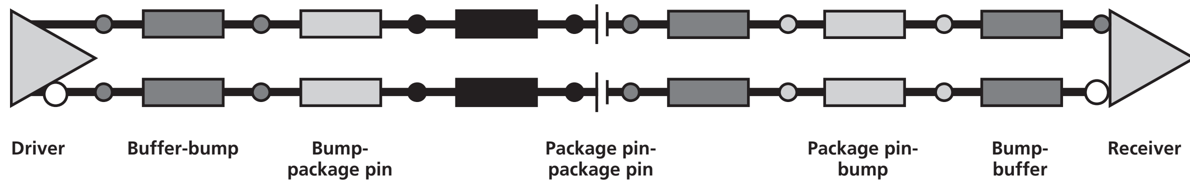

Figure 6: A point-to-point differential interconnect with in-series termination on the PCB

Even this simplest example demonstrates the complexity of interconnect design. At least four of the different elements shown in *Figure 6* are designed by different designers—working in dissimilar design domains—and implemented using different materials and feature sizes. Consider:

- The driver and receiver buffers are designed by the I/O buffer designer. Today's buffers are highly complex as more intelligence is added in the forms of pre-emphasis, de-emphasis, and equalization. These more intelligent buffers are designed to compensate for the noisy and lossy channels through which they need to drive a signal. One thing is certain—these designs are not getting any easier
- The buffer-bump segment of the interconnect is implemented by an IC designer in the final stages of IC design using an RDL of metal on the IC. The bump will be attached to the package substrate using a flip-chip or wirebond technique
- The bump-package pin segment is implemented by the IC package designer in the substrate of the IC package. There may be multiple signal and power layers in the package substrate. For complex devices, a BGA approach is the most common PCB attachment technique
- The package pin-package pin segment is implemented in the PCB or across multiple connectors and PCBs, which will be multilayered with signal and power planes to contend with

The problems created by this mismatch in fabric materials and feature sizes of the system components manifest in two key challenges: ensuring consistent impedance matching and managing signal loss across the interconnect within the allowed timing budget.

6.3 DEVELOPING THE VSIC MODEL

During the product development cycle, a product must first be “specified” or defined. The VSIC model is developed in the “explore” stage of the design process, during which technology options and choices are examined and selected and a set of design metrics is developed (*see Figure 7*). During the “design” phase, to determine shared design metrics, the designer—in this case a system integrator—will look at feasibility options, solution space options, and capture and bind constraints to the interconnect. The integrator will have to budget delay between the different interconnect segments and design a topology that satisfies timing, signal quality and, ultimately, the desired bit error rate (BER). During “implementation,” design layout occurs. Once the design database is “verified,” the product can be manufactured.

Figure 7: The product development cycle, from specification to manufacture

6.4 CREATING THE VSIC MODEL

To begin defining the VSIC model, the integrator first determines which (if any) of the interconnect segments are fixed, i.e. they already exist. For example, one of the ICs may be off the shelf or the PCB may plug into an existing backplane. Fixed segments are not subject to change and will therefore constrain the remainder of the components to be designed. If the design has fixed segments, the integrator will first set up models for those segments. For the following discussion, we assume that all segments of the interconnect will be designed.

Next, the integrator creates models for the required behavior of the buffers if they need to be designed (sometimes I/O buffers are fully characterized as part of an existing IC design or as part of an IP library). These models will act as specifications for the I/O buffer designer. Even though the I/O is not designed, a behavioral model can be created to drive circuit simulation of the system interconnect.

Now the integrator is ready to explore options for the topology itself, taking into account the electrical properties of the interconnect materials as well as the logical, electrical, and physical requirements. Physical requirements include die-size/shape/orientation versus package cavity; routability; package footprint to board; and, form factor of the end product. Electrical aspects include timing; signal integrity; loss; power distribution; and I/O modeling and analysis.

Finally, the integrator will physically floorplan the interconnect understanding the minimum and maximum timing delays and distances that must be supported in order for this interconnect to be physically implementable. Thermal and power delivery system requirements must also be factored in. This floorplanning will provide a start for the downstream IC package and PCB design.

In summary, the deliverables from the systems integrator for the exploration stage include:

- Buffer models that specify the required behavior of the buffers to be implemented by the I/O buffer designer
- Topologies that define the electrical constraints of the different elements of the interconnect. Appended together, they define the overall electrical constraints for the interconnect from buffer to buffer
- Initial floorplanning that can be used as a starting point for the IC package and PCB design

6.5 USING THE VSIC MODEL

All of the work the system integrator has done is captured as a set of appended topologies for each of the five segments; there is also a master topology that captures the entire system interconnect design intent. Once complete, the various segments are distributed to the team—the I/O buffer designer, the IC designer, the IC package designer, and the PCB designer.

6.5.1 I/O buffers tested within VSIC model

The I/O designer uses the buffer models as a specification for designing the I/O buffer circuit. It is designed and its behavior tested within the VSIC model. As the package and PCB are designed, the VSIC model can be updated with actual design data so the I/O designer can validate the buffer models against actual package and board implementations. If there is a problem and the designer is unable to satisfy the parameters assigned in the VSIC model, then he or she will negotiate with the integrator to solve it.

When the design is complete, the designer provides the integrator with an actual transistor model of the buffer, updating the VSIC model. In the interest of simulation performance, a behavioral model that accurately represents the transistor model over the desired operating regions can be provided. The designer should correlate the behavioral model with the transistor model to verify accuracy.

6.5.2 The IC designer and package designer optimize IC bump pattern

The IC designer places the I/O buffer cells in the IC in a multifaceted process. Relative to the system interconnect, the designer needs to ensure that the bump array pattern can actually be implemented in the package design. In order to do this, the designer needs a process whereby the bump pattern can be communicated to the IC package designer, who can then verify it will work. The co-design methodology calls for an automated process within the design environment to optimize the bump pattern for packaging. Once the bump pattern is defined and the RDL is created, the designer must ensure the VSIC model is updated to reflect the actual design.

If the IC designer runs into problems, negotiations are conducted with the system integrator. For example, if the allotted timing budget cannot be met, the designer executes with the minimum delay feasible and then conveys the information to the integrator. The new information is built back into the master VSIC topology and the integrator re-budgets the delay for the rest of the interconnect segments. In this manner, problems are discovered and addressed early in the design process.

6.5.3 IC package designer collaborates with IC and PCB designers

As previously discussed, the package designer needs the IC bump array information from the IC designer as early as possible in the co-design process in order to ensure a package can be designed successfully and economically. If the package designer discovers that the package will not work due to congestion, for example, the co-design methodology proposes an automated process to communicate with the IC designer so a change may be requested or an alternate bump pattern suggested. An industry-standard database such as OpenAccess would provide a good channel for this exchange.

Once the package designer and the IC designer have decided on a final bump pattern, the package designer proceeds with package design according to the VSIC model constraints. Now the package designer can work with the PCB designer to successfully implement the package onto the board.

6.5.4 PCB designer and IC package designer reduce prototype spins

The PCB designer uses the package-pin to package-pin topology to implement the design, verifying the PCB segment of interconnect in the context of the master topology. To avoid costly redesign, the PCB designer needs a communication link with the IC package designer to enable collaboration on optimizing package-pin design for routing ease.

6.5.5 VSIC model ensures designers have access to the same data

In review, the ability of designers to collaborate across design domains, make system level tradeoffs, and update the VSIC model so all designers in the flow are working with the same data can dramatically reduce iterations and help ensure first-time design success.

7 CO-DESIGN METHODOLOGY LINKS IC AND PCB SYSTEMS DESIGN

Finally, the co-design methodology links the IC and PCB domains by attacking an important bottleneck in multigigabit system interconnect design—the implementation of new silicon devices in a system. Once again, differing design environments, processes, and tools account for lengthy delays when PCB designers attempt to incorporate new silicon devices into their systems.

Today, IC producers attempt to address this problem with varying qualities of I/O models and written documentation telling users how to design interconnects that work with their devices. However, systems companies have to spend considerable time studying, interpreting, and testing in order to evaluate device performance. This can take weeks or months of effort for each complex device.

The co-design methodology speeds the process by enabling IC companies to provide users with a silicon design-in kit, i.e. an electronic blueprint for the implementation of silicon in a system. The IC manufacturer can now deliver a kit to systems companies when—or even before—new silicon is available. Designed to be plug-and-play compatible, design kits rapidly accelerate time to simulate and design-in complex devices. A good design-in kit can drive the entire design process from simulation and exploration to floorplanning, routing, and verification, enabling designers to remove weeks from the design cycle.

Importantly, in creating the kit, IC producers are able to re-use much of the system interconnect design work already done by the I/O designer, IC package designer, and PCB designer.

8 SYSTEM INTERCONNECT CO-DESIGN PLATFORM REQUIREMENTS

The new co-design methodology for system interconnect requires a new technology platform—one that supports the creation and updating of a VSIC model and enables collaboration across design domains from the beginning to the end of the design cycle (*see Figure 8*). It must support management of shared constraints throughout the process and address both the traditional logical and physical design issues, as well as the increasingly complex challenges of timing, power, and signal integrity. Importantly, the co-design environment must empower and inform each of the users in the flow, including the system architect, system integrator, I/O buffer designer, IC designer, IC package designer, and PCB designer as well as critical design chain team members.

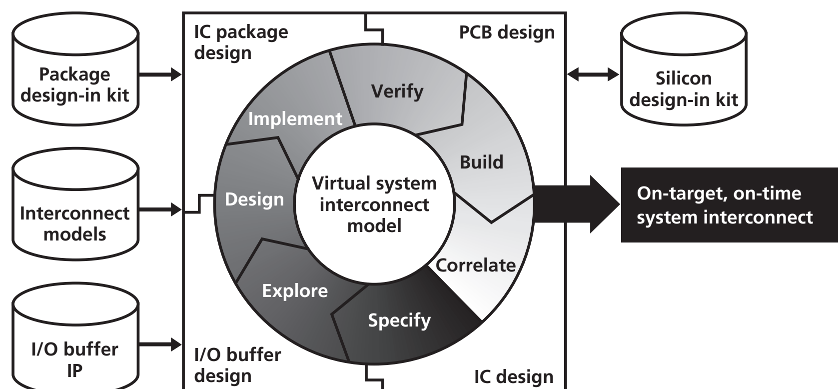

Figure 8: An integrated technology platform supports the VSIC model, IP availability, and silicon design-in technology

8.1 COMMON CO-DESIGN INFRASTRUCTURE CREATES FOUNDATION

There are two critical infrastructure requirements for supporting true system interconnect co-design: a common database and a shared constraint management system.

First, the technology platform must be built on a common physical database. A common database eliminates the need for data translations and enables implementation of the interconnect across design domains. The importance of a common database cannot be stressed enough because it permits co-design users within each domain access to the same data and freedom to update that data. Without a common database, the productivity and economic benefits of a co-design methodology cannot be realized.

Second, the platform must capture design intent in the form of constraints and manage those constraints in a common constraint management system that can be used by all designers and all tools in the flow. The lack of a common constraint management system will result in time-consuming translations and possible loss of meaning or errors in meaning as a constraint is passed from tool to tool or domain to domain.

8.2 OPTIMIZING THE SYSTEM INTERCONNECT DESIGN FLOW FOR CO-DESIGN

Referencing a simplified co-design flow (*see Figure 9*), the technology platform capabilities necessary to implement it will be discussed. Given a common database and shared constraint management system, we consider first the tools necessary for the creation of a VSIC model and the realization of a successful design. Key to the process is the production of accurate models.

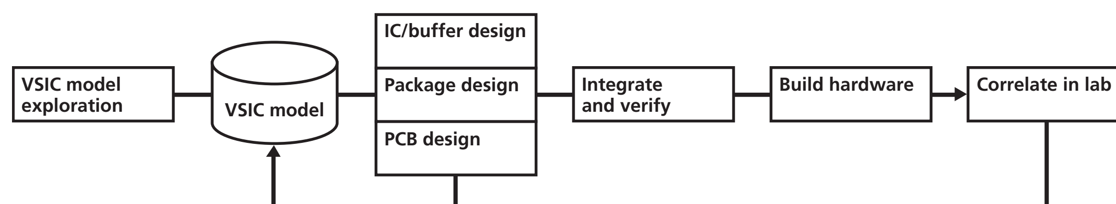

Figure 9: An effective co-design flow indicating feedback loop for updating the VSIC model

8.2.1 Creating accurate models

The VSIC model detailed in the methodology section consists of I/O models plus the interconnect model, constraints, and a floorplan that includes I/O-pin map, initial placement, and connectivity data. Obviously, to create an accurate system interconnect, the platform must enable both I/O models and interconnect models.

I/O modeling

Consider first I/O models; they are either created by the I/O designer or provided by a supplier such as an IP supplier or application-specific integrated circuit (ASIC) supplier. The co-design platform has to be able to simulate with both transistor-level and behavioral models. Ideally, the platform has advanced behavioral modeling capability that can be used until the standards, such as IBIS, evolve to address leading-edge designs. Advanced modeling and IBIS are used for a couple of reasons. First, they protect a manufacturer's IP associated with I/O circuit design when the model is provided to someone outside of the company. Second, they achieve much faster performance than SPICE transistor models—behavioral models are often hundreds of times faster. To reduce design cycles, the platform should enable designers to quickly create behavioral models from SPICE models.

With system speeds approaching multigigahertz levels, the need for faster simulation is mandatory. Designers now have to simulate with more and more bits in order to gain an accurate understanding of BER. By way of example, the PCI Express standard recommends that interconnect be simulated with at least 10,000 bits. A SPICE simulation cannot achieve this performance. Even now, many engineers working at these very high speeds are going back to building prototypes and measuring them in the lab with BER testers because of this simulation performance issue. In the future, the platform will need much higher simulation performance than is available today.

Interconnect modeling

The interconnect model is an electrical representation of all physical aspects of the interconnect including materials, bondwires, conductors, package pins and balls, vias, footprint pads, connectors, cables, and termination devices. It is created by the designers of the actual interconnect —the IC, package, and PCB designers. Typically the model is built using SPICE circuits and special models for transmission lines.

The co-design platform needs to allow for easy creation of these models either in a virtual form during exploration or for automatic extraction from actual physical designs. Again, as speeds approach multigigahertz levels, the platform will need to adopt more advanced modeling techniques for the interconnect such as S-parameters, 3D modeling of structures, and new, more accurate transmission line models.

8.2.2 Silicon design-in technology

As the co-design methodology recognizes the challenges faced by systems companies in implementing new silicon devices, so must the technology platform. To create an effective design-in kit the IC company needs a full-featured design and analysis solution that enables production of I/O buffer models; ready-to-simulate system-level topologies; large package models or actual package design; testbench and correlation data; constraint templates; an electronic reference PCB design including both schematic and constrained layout; and connector models for backplane applications and tutorials.

When provided to a systems company, silicon design-in kits jump-start the design-in process and remove weeks or months from the PCB systems design cycle.

8.2.3 Interconnect analysis

When the VSIC model is available, each of the designers can perform analysis of their piece of the interconnect. It is critical that the technology platform offer each co-design user the same analysis engine so consistent results are achieved. Analysis capabilities of the engine should support signal integrity, timing, and power delivery taking into account loss, crosstalk, reflections, and simultaneous switching noise (SSN) while sweeping a multitude of variables. The analysis needs to be backed up with solid reporting capabilities such as waveforms and eye diagrams. Future needs will include higher performance simulation and more support for analysis in the frequency domain.

8.2.4 The design phase

The logic design capture phase of the development process follows analysis. Here, the IC package designer needs to capture the connectivity between the package and the IC. This process could be automated or interactive depending on the state of definition of the bump array and package. Either way, it should involve some collaboration between IC designer and package designer to ensure optimal performance. This collaboration should be enabled by the platform through tight integration and ECO processes.

Logical design capture of the PCB usually takes the form of a schematic and is performed by the PCB designer. The co-design platform needs to ensure that schematic capture is integrated with the constraint management system. On the bleeding edge, high pin-count devices will demand more advanced design capture methods and the platform must be flexible enough to provide for them. Highly advanced devices can render a schematic almost useless from a documentation point of view so tools such as table-driven design capture must be supported, ensuring again that they are integrated with the constraint management system.

The physical design of the interconnect should also be integrated with the constraint management systems as well as being "electrically aware," meaning that as the interconnect is implemented, the interactive functions of the tool obey the constraints with real time checking while the automatic tools strive to be correct by construction.

The technology platform must, again, be flexible enough to accommodate more automation, especially in respect to the router. As more and more nets become constrained, it becomes more and more difficult to achieve 100 percent router completion while satisfying those constraints. As a result, designers are often forced to use interactive functions to complete the job. Today's autorouters must advance to the next level where they can complete these tough, highly constrained designs.

8.2.5 Post layout verification

Once the interconnect has been implemented, verification must be performed before actual hardware can be built. The platform must promote use of the same models, analysis, and simulation engines that were used earlier in the methodology to ensure consistency of results. Extraction of the interconnect models should be automated and analysis should take into account actual crosstalk caused by the implementation of the routing and real-world manufacturing tolerances. Again, as designs are getting faster and denser, higher performance simulation and accurate modeling will be required and the co-design platform must be flexible enough to deliver.

9 CONCLUSION

Market demand for compact, high-performance products is driving manufacturers to pack more functionality into smaller devices creating unprecedented design challenges in the areas of density, speed, and power delivery. To remain competitive, manufacturers are looking for ways to reduce design costs and design cycle times.

The new co-design methodology discussed in this paper enables producers of electronic products to cut both their design costs and time to market. Supported by a unique technology platform, the new methodology enables engineers to co-design an IC, its package, and the PCB simultaneously, optimizing the system interconnect.

Many companies will be able to remove weeks or months from the design process with the combination of best practices and deployment of the proposed co-design methodology and associated technology platform. Cost savings are realized through eliminating or reducing design iterations between the IC, IC package, and PCB design domains as well as within the domains; reducing the risk of IC mask re-spins; reducing the cost of the IC package and eliminating package re-spins; accelerating the time it takes to successfully design-in a complex IC; and reducing the number of PCB prototypes before the board is ready for production. These are not efficiencies that can be realized using today's disparate, dissimilar design environments. Clearly, system co-design is a methodology whose time has come.

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